

A Mix-Control Drive Method for Passive Matrix OLED

TANG Zhi-jie¹⁾, RAN Feng²⁾, XU Mei-hua¹⁾

¹⁾ (Key Laboratory of Advanced Displays and System Application, Ministry of Education, Shanghai University, Shanghai 200072)

²⁾ (Microelectronic Research and Development Center, Shanghai University, Shanghai 200072)

Abstract A mix-control driving method of passive matrix OLED (PM-OLED) is described to drive high gray scale display. The method is based on mix-control of current digital-to-analog converter (DAC) and digital space-time modulation (DSTM). The low-bit gray scale is driven by the DAC while the high-bit gray scale is generated by DSTM. This method is applied to a 128 × 128 dots RGB PM-OLED panel which can drive 512 gray scales.

Keywords PM-OLED, gray scale, space-time modulation, current DAC

一种被动矩阵 OLED 的混合控制驱动方法

唐智杰¹⁾ 冉峰²⁾ 徐美华¹⁾

¹⁾ (上海大学新型显示国家重点实验室, 上海 200072) ²⁾ (上海大学微电子研究开发中心, 上海 200072)

摘要 本文介绍一种用于实现被动有机发光二极管矩阵 (PM-OLED) 高灰度显示的混合驱动方法。该方法基于电流型数模转换器和时空数字调制方法的混合驱动来实现整体屏幕的显示驱动。在该方法中, 显示数据的低灰度权值由数模转换器完成调制, 同时显示数据的高灰度权值由时空数字调制方法进行调制。该方法应用于 128 × 128 彩色 PM-OLED 可以驱动 512 级灰度显示。

关键词 PM-OLED 灰度 时空调制 电流型数模转换器

中图分类号: TN873 **文献标识码:** A **文章编号:** 1006-8961(2006)11-1534-05

1 Introduction

Organic light emitting displays (OLEDs) have been particularly attractive in potential applications of flat panel displays (FPDs) because of their low cost, high brightness, wide viewing angle, fast response time, low operating voltage, and very thin thickness^[1-3].

Because the OLEDs are controlled by the current, the luminance of the OLEDs is proportional to the magnitude of the current applied to each pixel. There are two current driving methods to realize the gray scale modulation^[4,5]. Pulse amplitude modulation (PAM)

method modulates the current amplitude to modulate the gray scale. Pulse width modulation (PWM) method modulates the lighting time with a constant current through the pixel. Both of them drive the gray scale by changing the efficient current flowing into the pixels. The larger the efficient current is, the lighter the pixel dot is.

In order to improve OLED display quality, we must enhance gray scale. Then the PAM needs higher accurate current amplitude scale while the PWM needs higher scan frequency. Then, all of them will make many difficulties to the system realization about the high accurate current digital-to-analog converter (DAC) and high system drive clock.

收稿日期: 2006-06-25; 改回日期: 2006-08-20

第一作者简介: 唐智杰 (1977 ~), 男, 2005 年获得上海大学硕士学位, 现为上海大学博士研究生。主要从事 OLED 和 TFT-LCD 的驱动方法研究及其芯片实现。E-mail: joviertang@163.com

This paper reports a mix-control drive method for passive-matrix OLED (PM-OLED) which can improve gray scale with lower accurate current DAC and lower scan frequency. It uses digital space-time modulation cooperating with the current DAC to generate the high gray scale.

2 Principle of proposed drive method

2.1 System Principle

We divide the display data of a pixel into two parts (low-bits and high-bits). The low-bits of a pixel are driven by current DAC of column driver IC (integrated circuit) while the high-bits are scanned by digital space-time modulation (DSTM) in OLED controller IC. In the system shown in Fig. 1, there are three ICs (OLED controller, column driver and row driver) and PM-OLED display panel. The display data are transported from micro processor unit (MPU) to controller IC. According to the DSTM, the controller IC generates the driving control timing, address and data for column driver IC and row driver IC. The column IC decodes the address data and latches the corresponding low-bits of the pixel data, which are DAC converted to drive output. The row address is decoded to drive the corresponding row of the panel.

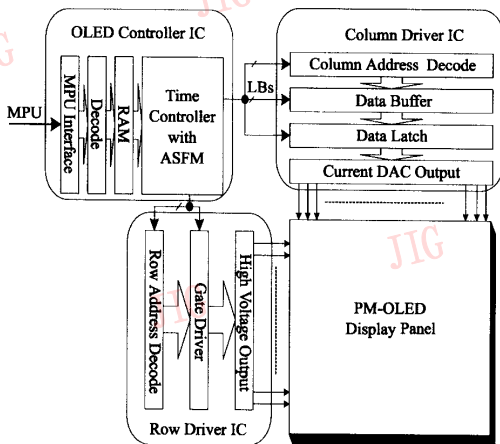


Fig. 1 System architecture of Mix-control gray scale drive

2.2 Current DAC design

There is a 4-bit current DAC for every column

output drive in the column driver IC. The current DAC is designed with Cascode current mirror and differential amplifier^[6]. The drive source voltage (VDD) is 9V. The logic voltage is 3.3V and the range of the drive current output is from 100μA to 1.5mA.

The schematic of the Cascode current mirror DAC is shown in Fig. 2.

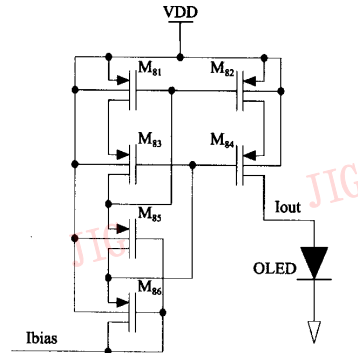


Fig. 2 Circuit diagram of Cascode current mirror

The Cascode current mirror consists of the mosfet device M₈₁ ~ M₈₆. In these devices, M₈₅ and M₈₆ generate the bias voltage to Cascode current mirror.

The mirror bias source current is provided by the mosfet device M₁ and differential amplifier. The circuit diagram is shown in Fig. 3. The bias current can be micro-adjusted by the bias voltage of VB₁ and VB₂.

The current output is simulated by hspice shown in Fig. 4.

2.3 Digital space-time modulation (DSTM)

With the traditional PWM, the gray scale can be achieved by controlling the frame valid driving time (1-2-4-8—2ⁿ-1) according to the bit power (B₀-B₁-B_{n-1}) of the pixel data. The gray value of a pixel X is shown in the formula(1).

$$G_x = B_0 \times 2^0 + B_1 \times 2^1 + \dots + B_{n-1} \times 2^{n-1} \quad (1)$$

For example, to an 8 level gray scale scan, it divides a scan cycle to 8 time slices (cycles), then it achieves different gray scale by turning on or turning off pixel current during the corresponding cycle shown in Tab. 1.

In the Tab. 1, the C_n means the sequence number of the drive cycles. The G means the gray value and

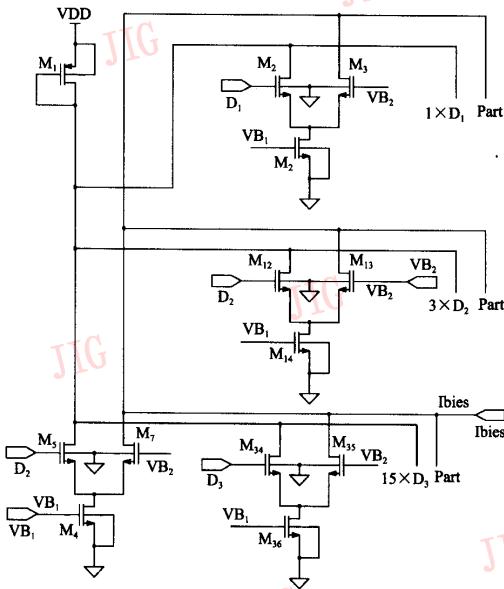


Fig. 3 Circuit diagram of 4-bit controllable bias current

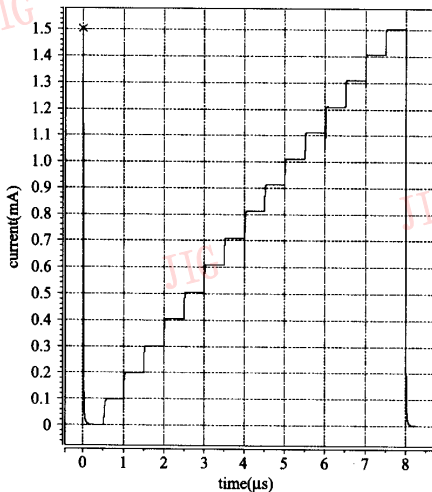


Fig. 4 The current DAC output characteristic

Tab. 1 PWM modulation of 8 gray scales

G_n	1	2	3	4	5	6	7	8
G, B	B_0	B_1	W	B_2	W	W	W	B_x
1	█							
2	█	█						
3	█	█	█					
4	█	█	█	█				
5	█	█	█	█	█			
6	█	█	█	█	█	█		
7	█	█	█	█	█	█	█	
8	█	█	█	█	█	█	█	█

the B means the bit power of the display data. And the B_x means the vanishing cycle. From the Tab. 1, we can see that during the 8 cycles, the available scanning cycle number is $4(B_0, B_1, B_2, B_x)$, while the other times are waiting cycles (shown as W).

Then the drive efficiency E_d is:

$$E_d = \frac{T_d}{T_{all}} = \frac{4}{8} = 50\% \quad (2)$$

Then we can analogically calculate the drive efficiency of other gray scales, shown in Tab. 2.

Tab. 2 The drive characteristic of traditional modulation

Gray Scale	8	32	64	256	512
$E_d(\%)$	50	18.75	10.94	3.52	1.95
Minimum Clock (MHz)	2.95	11.80	23.59	94.37	188.74

To a scale of 128×128 dots RGB PM-OLED panel, the minimum data drive clock values are also shown in Tab. 2 according to the formula (3) while the frame frequency F is 60Hz and DataWidth is 8. Data width means the bit number of the transport display data in a system clock.

$$clk = \frac{Columns \times Rows \times GrayScale}{DataWidth} \times F \quad (3)$$

From the Tab. 2, we can see that with the gray scale increasing, the traditional PWM drive efficiency drops horribly while the minimum clock value increases acutely. When the gray scale increases to 512, the data clock is too high to achieve for normal PM-OLED technology.

To a 2^n gray scale, the total available drive output cycle number is $n + 1$, and the waiting cycle number is $2^n - n - 1$. Then we enhance the drive efficiency using DSTM which can activate the waiting cycle by dividing the entire panel to S_N sub-partitions. Then we calculate the maximum sub-partition number S_N and drive sequence in order to maximize the E_d to attain about 100%. Then the drive efficiency is

$$E_d = \frac{T_d}{T_{all}} = \frac{S_N \times (n + 1)}{2^n - 1 + S_N} \quad (4)$$

Let $E_d = 100\%$, then we get:

$$S_N = \frac{2^n - 1}{n} \quad (5)$$

The drive clock can be calculated by:

$$clk = \frac{Columns \times Rows \times (2^n - 2 + S_N)}{DataWidth \times S_N} \times F \quad (6)$$

Then we calculate the drive efficiency by formula (4) and the minimum data drive clock values by formula (6) for a 128 × 128 dots RGB PM-OLED panel at the same conditions (frame frequency F is 60Hz and DataWidth is 8) shown in Tab. 3.

Tab. 3 The drive characteristic of DSTM

Gray Scale	8	32	64	256	512
S_N	2	6	10	31	56
E_d (%)	88.9	97.3	95.9	97.6	98.8
Minimum Clock (MHz)	1.66	2.27	2.69	3.40	3.73

From the Tab. 3, we can see that the drive efficiency has been improved and the minimum data drive clock drops sharply. Then the DSTM is easy to be realized for traditional logic devices and normal PM-OLED technology.

The drive sequence of 32 level gray scales DSTM (sub-partition number $S_N = 6$) is shown in Tab. 4.

From the Tab. 4, there is only 1 ineffective drive cycle ($C_n = 15$) while the other 36 cycles are all available. Then the drive efficiency is:

$$E_d = \frac{T_d}{T_{all}} = \frac{36}{37} = 97.30\% \quad (7)$$

This drive efficiency is much higher than that of the traditional PWM according to Tab. 2.

3 Realization and Discussion

We design the drive system for a 128 × 128 dots RGB PM-OLED using mix-control drive method. The system clock is set to 15MHz, while the DSTM drives the high 5 bits gray display according to Tab. 4 and the current DAC drives the low 4 bits gray display. The entire panel is divided into 6 sub-partitions according to Tab. 3. The data width is set to 8 bits, which are used to transport the low 4 bits of two columns. The display gray scale is $2^{5+4} = 2^9 (512)$. The maximum frame frequency is:

Tab. 4 DSTM drive sequence of 32 gray scales display

C_n	P_1	P_2	P_3	P_4	P_5	P_6
1	B_4					
2		B_4				
3			B_3			
4				B_2		
5					B_2	
6						B_0
7						B_3
8				B_4		
9					B_0	
10					B_2	
11			B_1			
12						B_3
13				B_0		
14				B_4		
15						
16						B_2
17	B_1					
18		B_3				
19	B_2					
20						B_1
21					B_4	
22						B_4
23	B_8					
24				B_0		
25				B_1		
26			B_1			
27				B_3		
28		B_0				
29		B_2				
30			B_2			
31	B_0					
32	B_x					
33		B_x				
34			B_x			
35				B_x		
36					B_x	
37						B_x

$$F_{max} = \frac{SysClock \times N_p \times S_N}{Columns \times Rows \times (2^n - 1 + S_N)}$$

$$= \frac{15 \times 10^6 \times 2 \times 6}{(128 \times 3) \times 128 \times (2^5 - 1 + 6)} = 99.0\text{Hz} \quad (8)$$

In the formula (8), N_p means the transport column number in a system clock. Then we can see that we realized the high gray scale (512) display which can receive satisfying display quality only with 15MHz system clock and 4-bit current DAC. If we

realize the same high gray scale, the traditional PWM needs 311.43MHz according to formula (3) and the PAM needs 9-bit current DAC.

DSTM can be used not only for PM-OLED but also for AM-OLED because they have the same scan mode.

4 Summary

The circuit simulations and system realization indicate that the mix-control drive method can easily realize the high gray scale drive for PM-OLED with lower system data drive clock and low bit DACs.

In addition, because DSTM is a digital process, we can add the additional functions such as display data Gamma rectification and display scaling into it.

Acknowledgments The authors would like to acknowledge the financial support from the Foundation of Shanghai Municipal Education Commission under grant No. 05ZZ03, and also to acknowledge the International Cooperation Foundation of Shanghai

Science and Technology Department for providing financial support for this work under grant No. 055207041.

References

- 1 Tang C W. An overview of organic electroluminescent materials and devices[J]. *Journal Society of Information Display*, 1997, 5(1): 11 ~ 14.
- 2 Tang C W, VanSlyke S A, Chen C H. Organic electroluminescent diodes[J]. *Journal Application Physical Letter*, 1987, 51(12): 913 ~ 915.
- 3 Gu G, Burrows P E, Venkatesh S, *et al.* Vacuum-deposited, no polymeric flexible organic light-emitting devices[J]. *Optics Letter*, 1997, 22(8): 172 ~ 174.
- 4 Gu G, Forest S R. Design of flat-panel displays based on organic light-emitting devices [J]. *IEEE Journal of Selected Topics in Quantum Electronics*, 1998, 4(1): 83 ~ 99.
- 5 Nathan A, Kumar A, Sakariya K, *et al.* Amorphous silicon thin film transistor circuit integration for organic LED displays on glass and plastic[J]. *IEEE Journal of Solid State Circuits*, 2004, 39(3): 1477 ~ 1486.
- 6 Balmford R A H, Redman-White W. New high-compliance CMOS current mirror with low harmonic distortion for high-frequency circuits [J]. *Electronics Letter*, 1993, 29(2): 1738 ~ 1739.